T0220T-66TSh00T

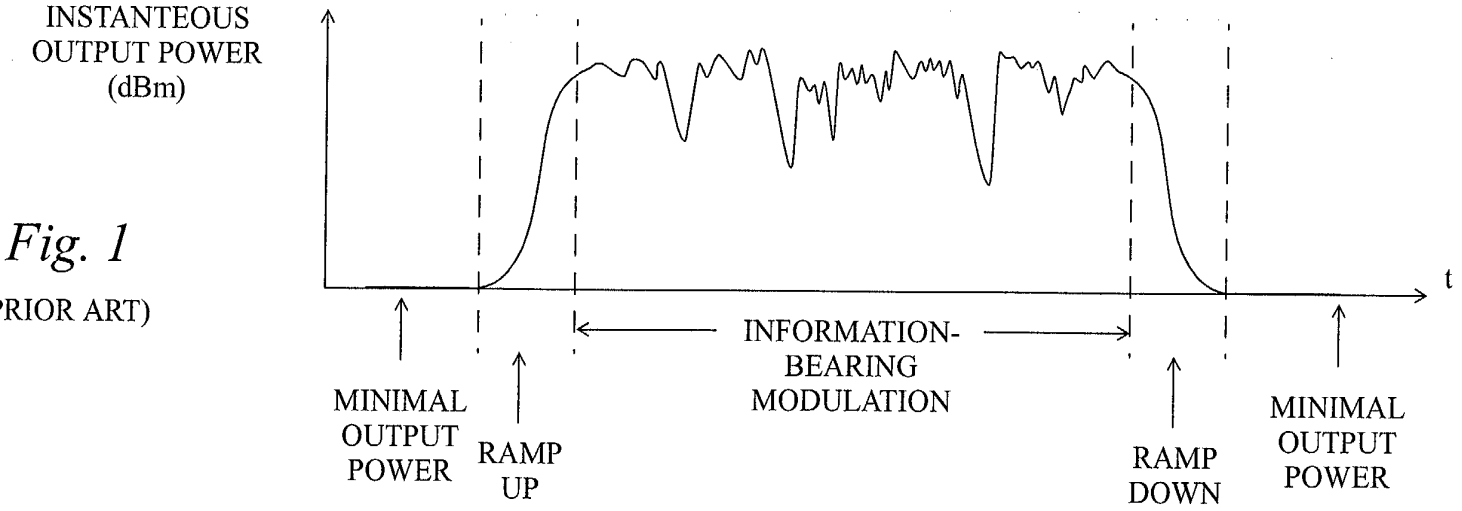


Fig. 1

(PRIOR ART)

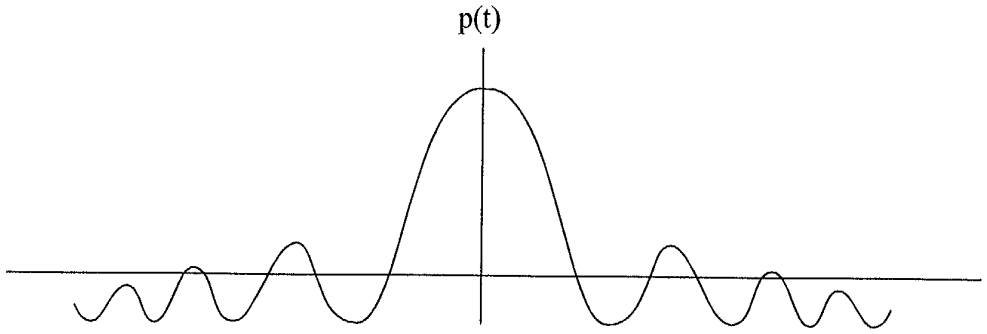


Fig. 13

(PRIOR ART)

T0220T "661Sh00T

Fig. 2
(PRIOR ART)

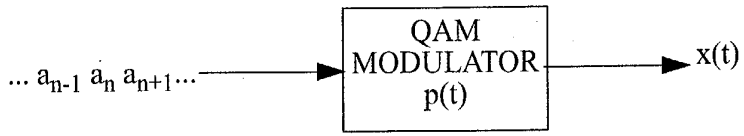


Fig. 3
(PRIOR ART)

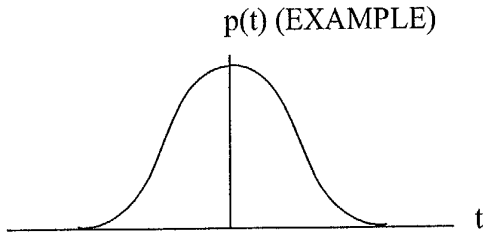
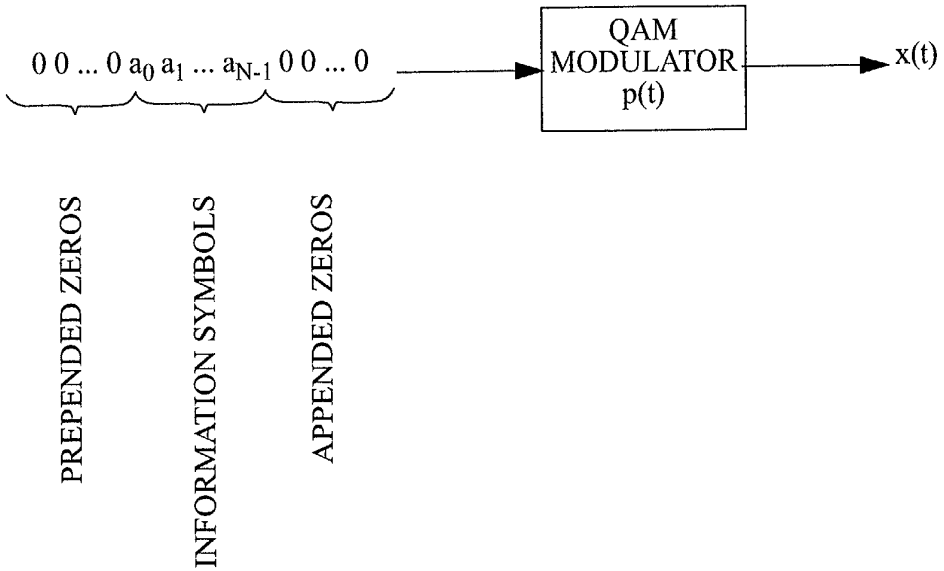
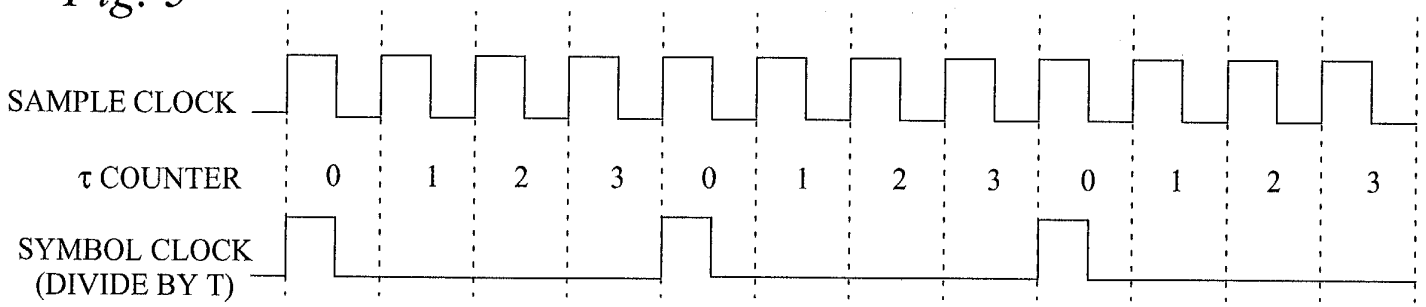


Fig. 4



TO220T "66TSh00t

Fig. 5



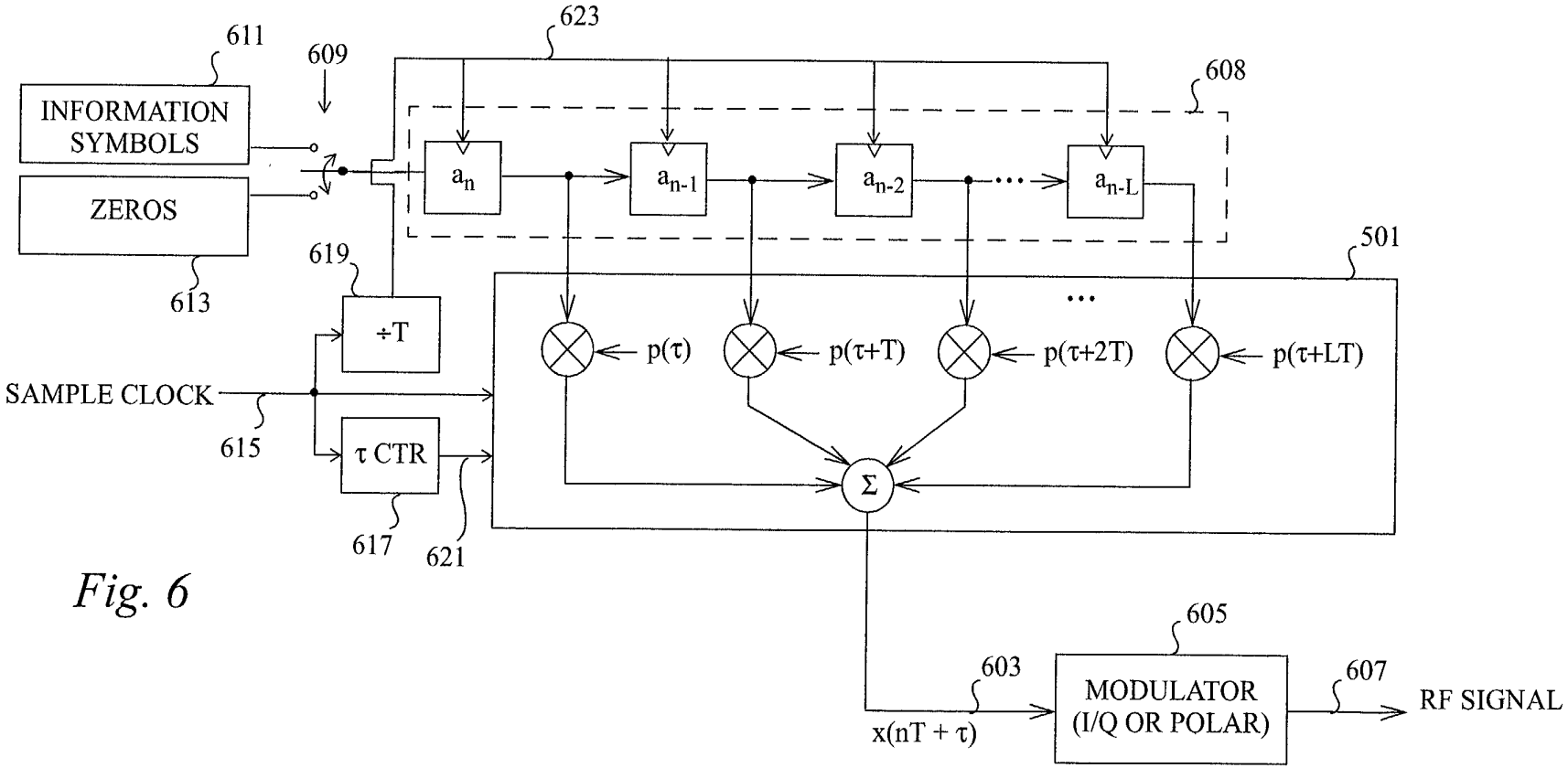


Fig. 6

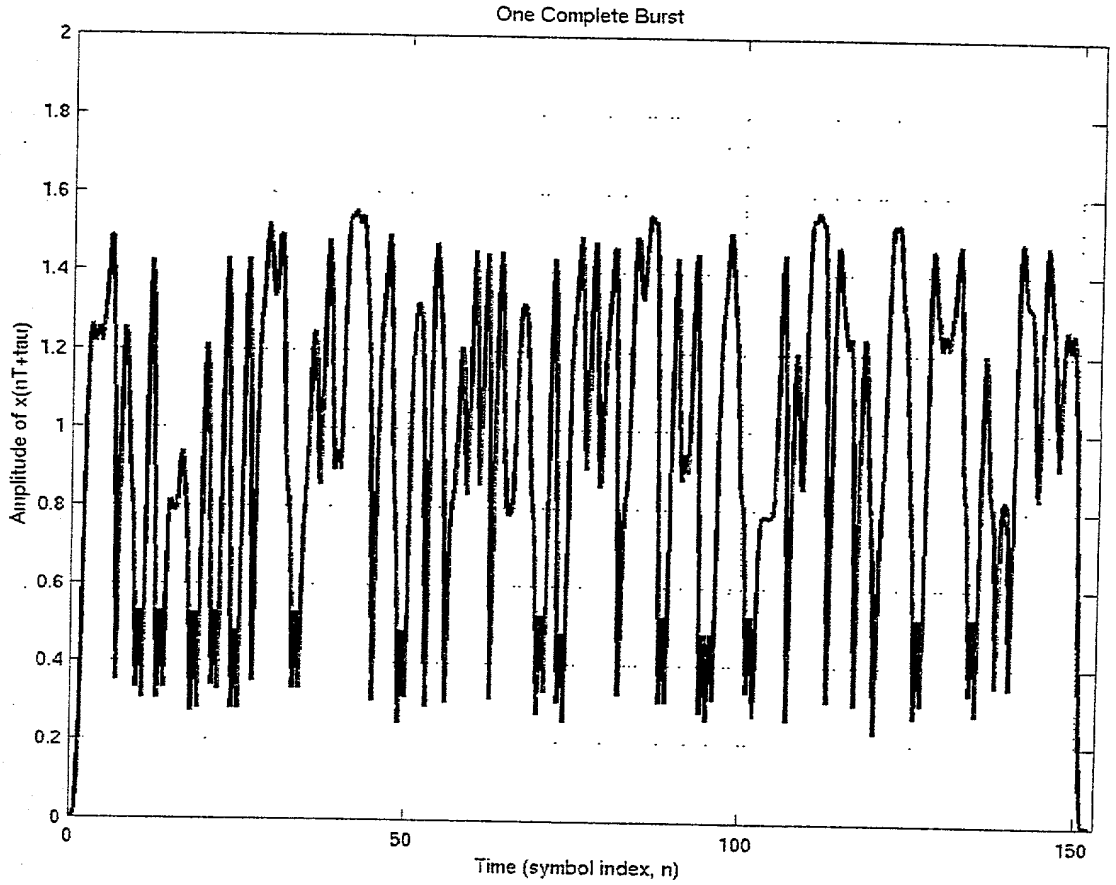

One Complete Burst
Amplitude of x(nT+tau)
Time (symbol index, n)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
0
50
100
150

Fig. 7

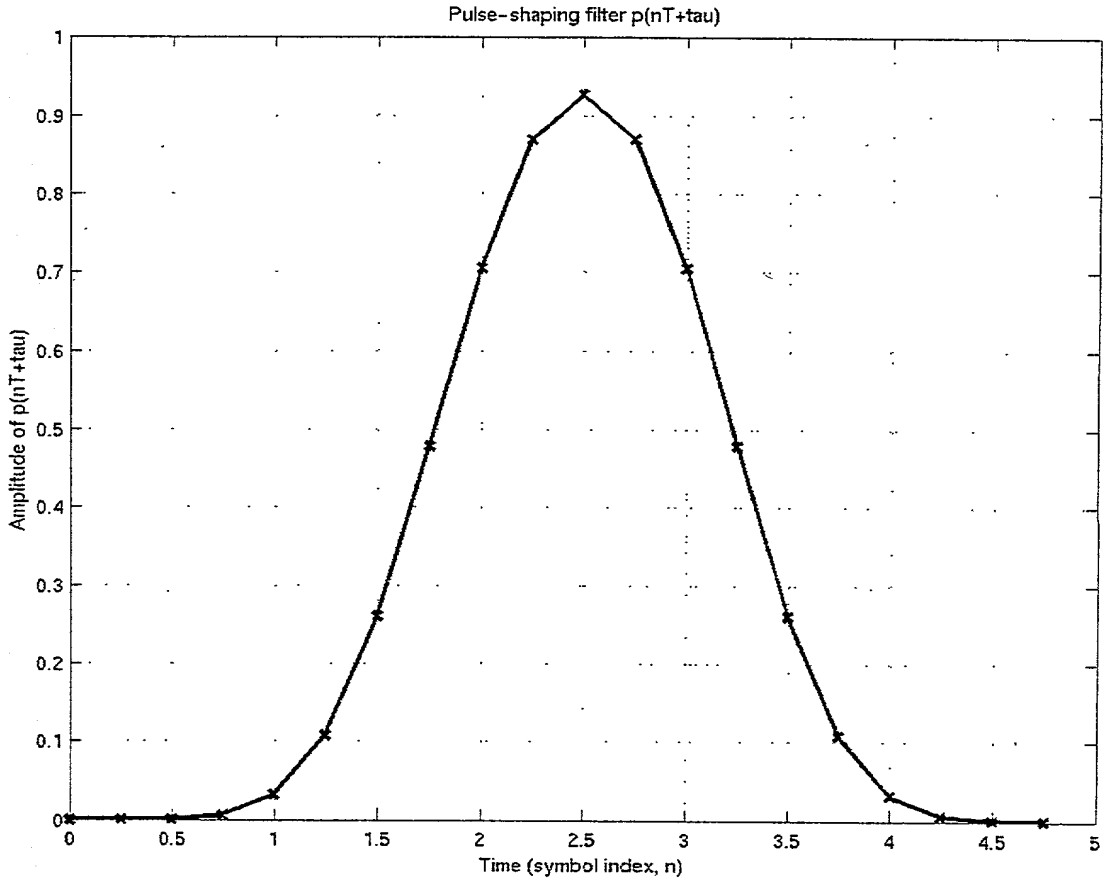
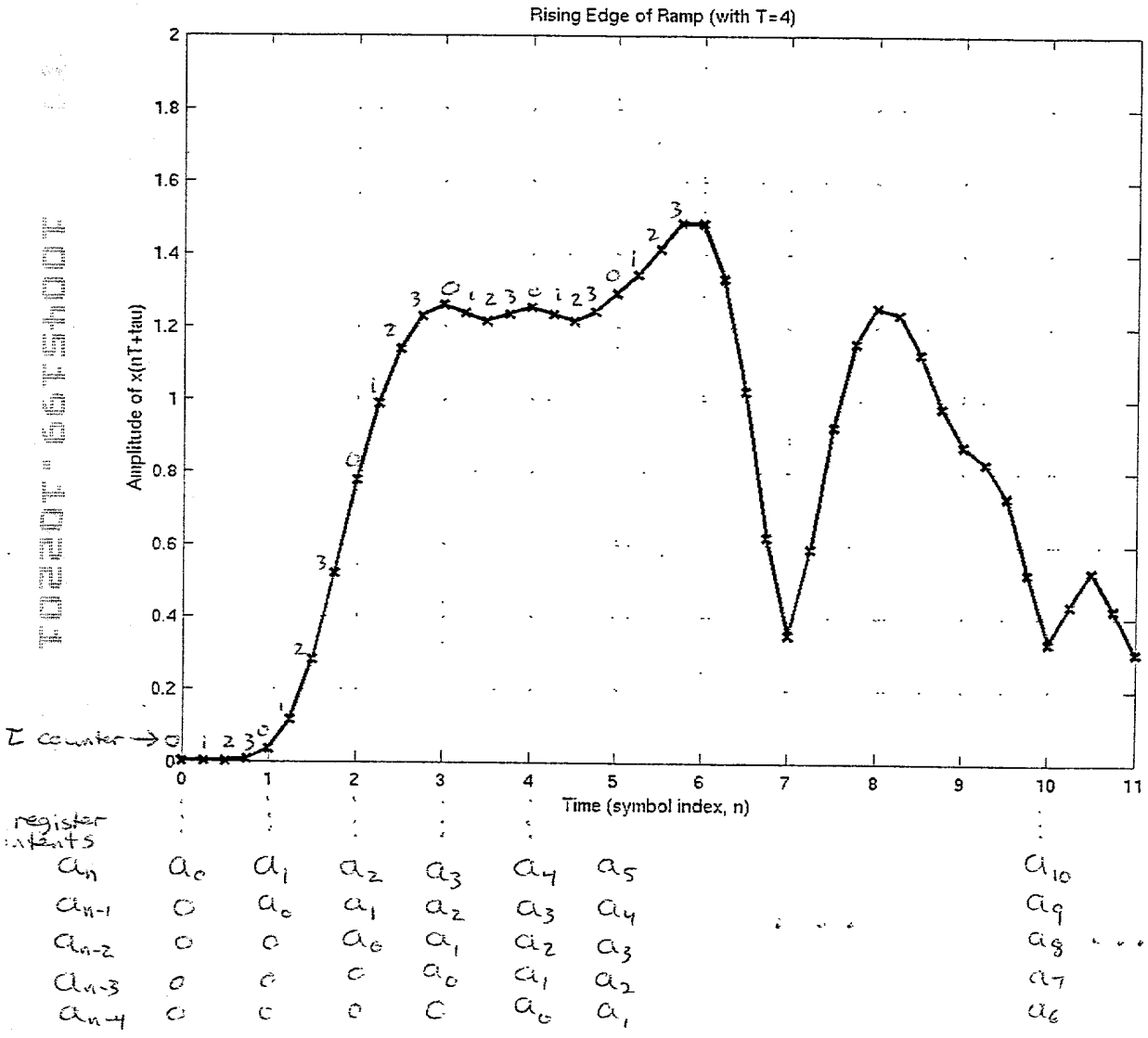

Pulse-shaping filter p(nT+tau)
Amplitude of p(nT+tau)
Time (symbol index, n)
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
0
0.5
1
1.5
2
2.5
3
3.5
4
4.5
5

Fig. 8



register contents

a_n	a_0	a_1	a_2	a_3	a_4	a_5	...	a_{10}
a_{n-1}	0	a_0	a_1	a_2	a_3	a_4	...	a_9
a_{n-2}	0	0	a_0	a_1	a_2	a_3	...	a_8
a_{n-3}	0	0	0	a_0	a_1	a_2	...	a_7
a_{n-4}	0	0	0	0	a_0	a_1	...	a_6

Fig. 9

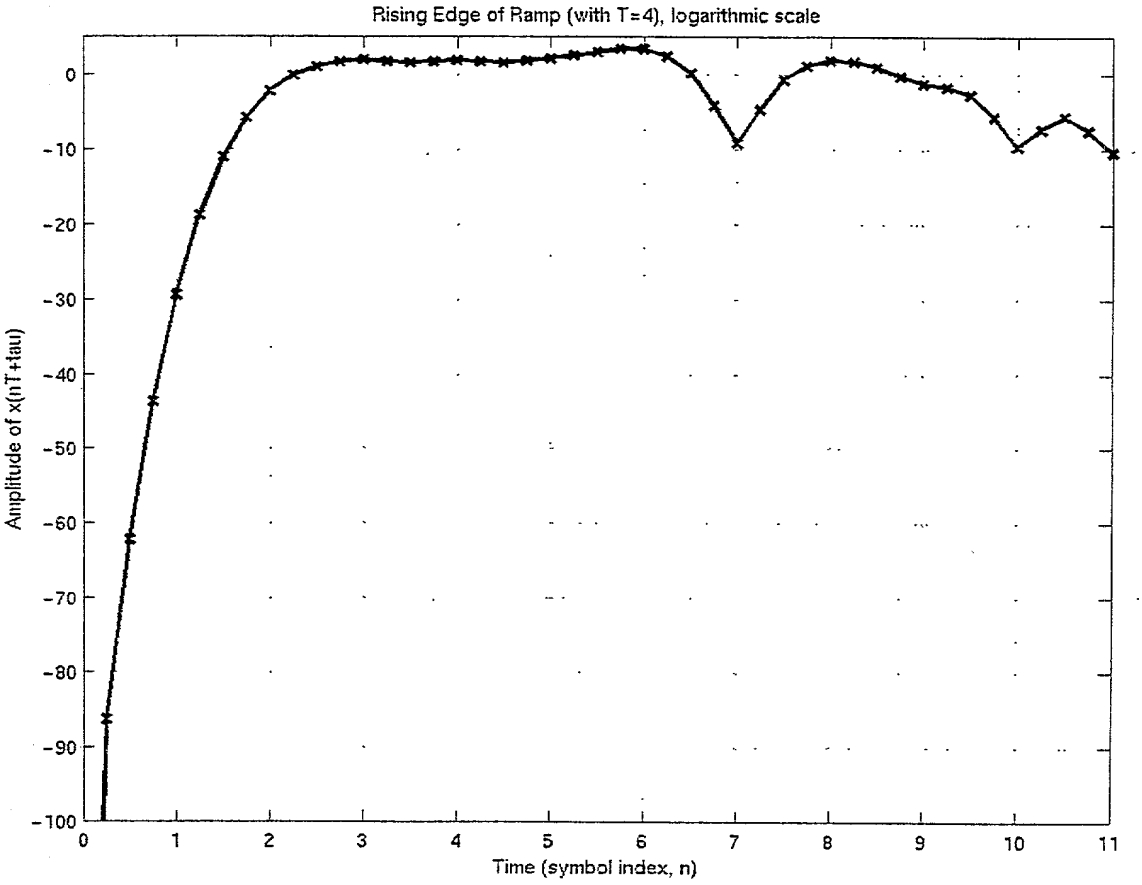
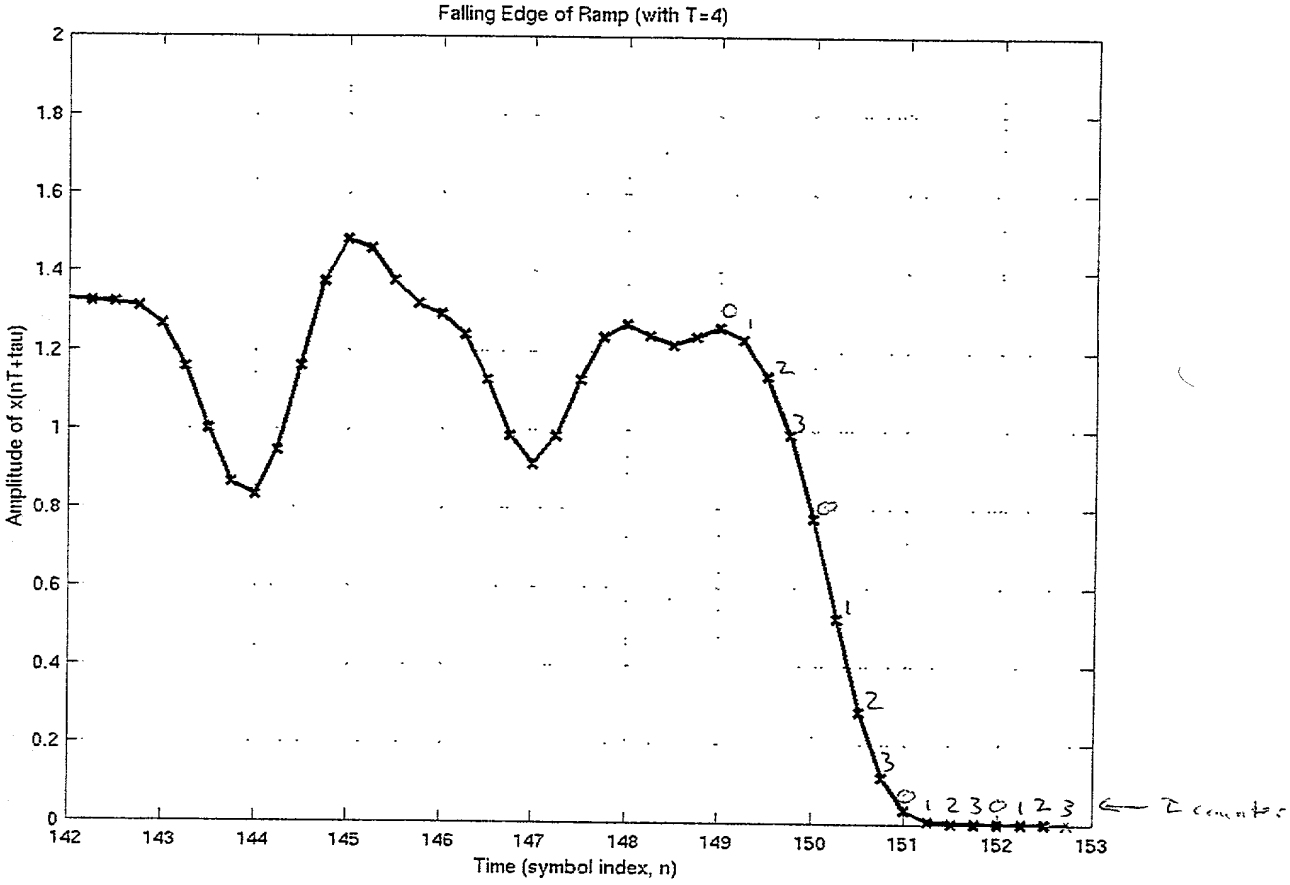

Rising Edge of Ramp (with T=4), logarithmic scale
Amplitude of x(nT+tau)
Time (symbol index, n)
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
1
2
3
4
5
6
7
8
9
10
11

Fig. 10



a_n a_{142}

a_{n-1} a_{141}

a_{n-2} a_{140}

a_{n-3} a_{139}

a_{n-4} a_{138}

a_{146} a_{147} 0 0 0 0 0

a_{145} a_{146} a_{147} 0 0 0 0

a_{144} a_{145} a_{146} a_{147} 0 0 0

a_{143} a_{144} a_{145} a_{146} a_{147} 0 0

a_{142} a_{143} a_{144} a_{145} a_{146} a_{147} 0

Fig. 11

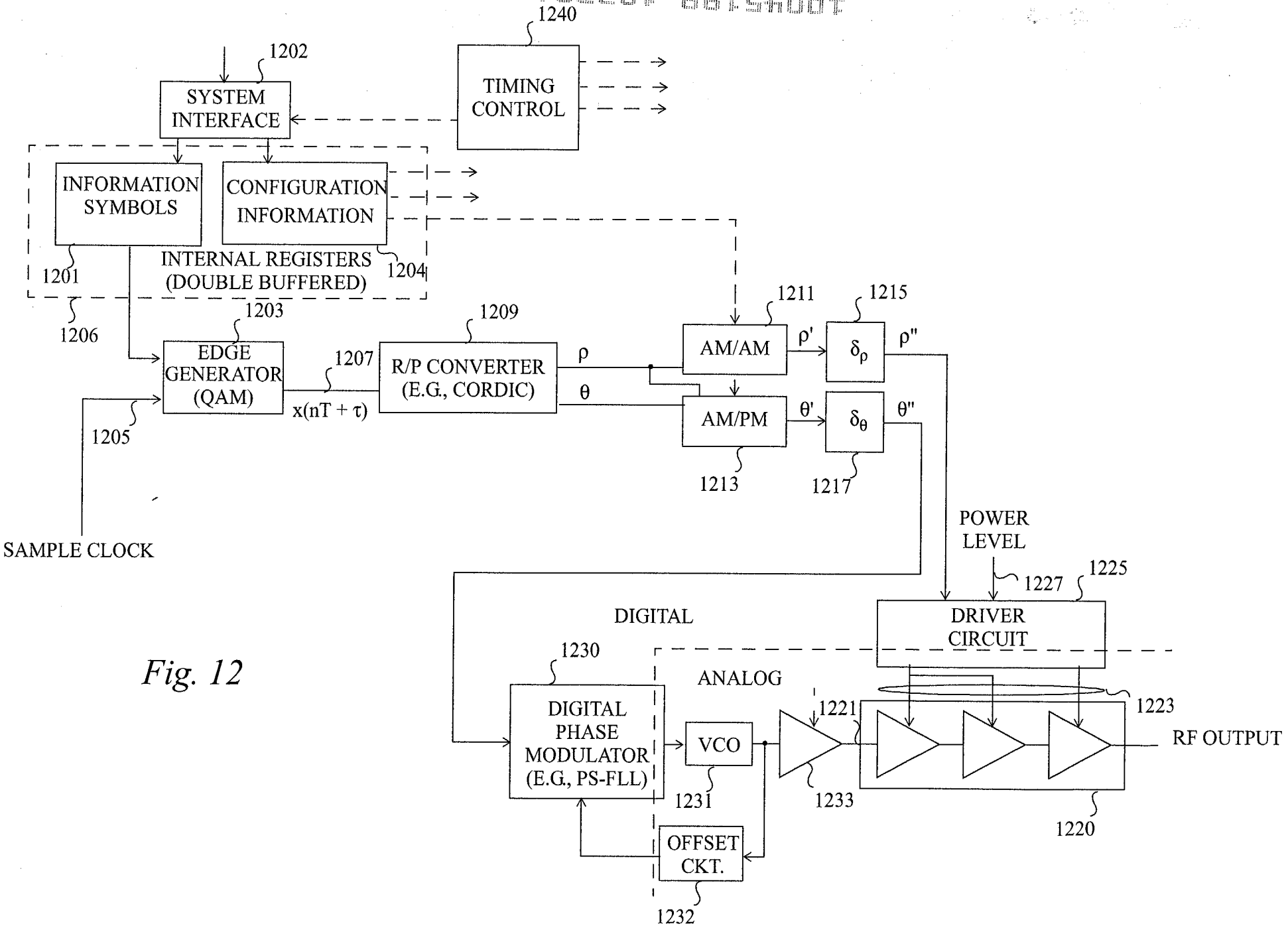

1240
1202
SYSTEM INTERFACE
TIMING CONTROL
INFORMATION SYMBOLS
CONFIGURATION INFORMATION
INTERNAL REGISTERS (DOUBLE BUFFERED)
1201
1204
1206
1203
1209
1211
1215
EDGE GENERATOR (QAM)
1207
R/P CONVERTER (E.G., CORDIC)
ρ
θ
AM/AM
ρ'
δ_ρ
ρ"
AM/PM
θ'
δ_θ
θ"
x(nT + τ)
1205
1213
1217
SAMPLE CLOCK
POWER LEVEL
1227
1225
DRIVER CIRCUIT
DIGITAL
ANALOG
1230
DIGITAL PHASE MODULATOR (E.G., PS-FLL)
VCO
1221
1223
RF OUTPUT
1231
1233
1220
OFFSET CKT.
1232

Fig. 12

TO220T "667SHOOT

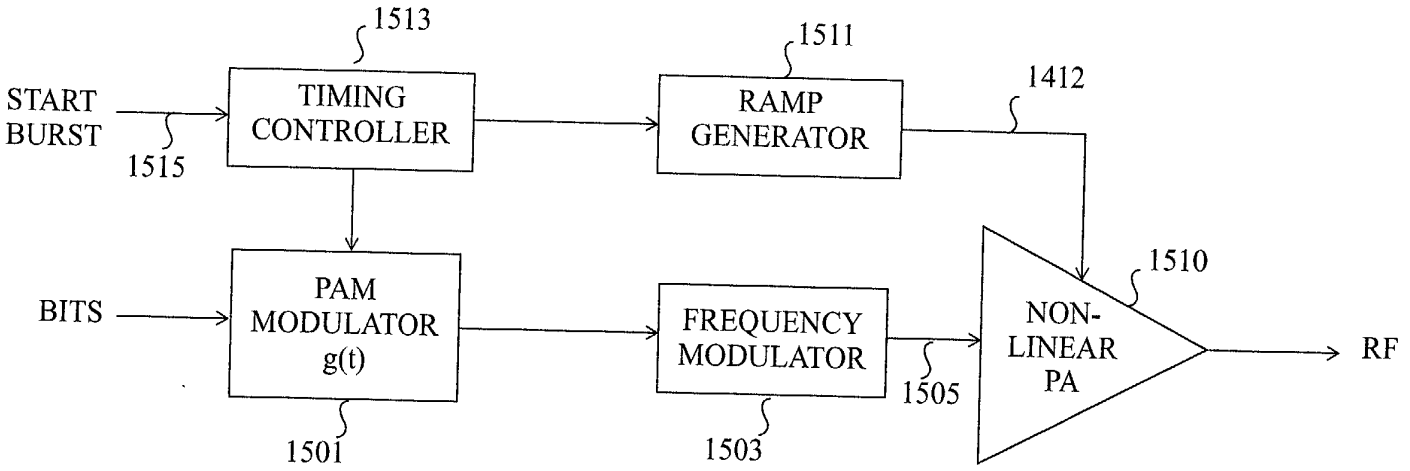


Fig. 15

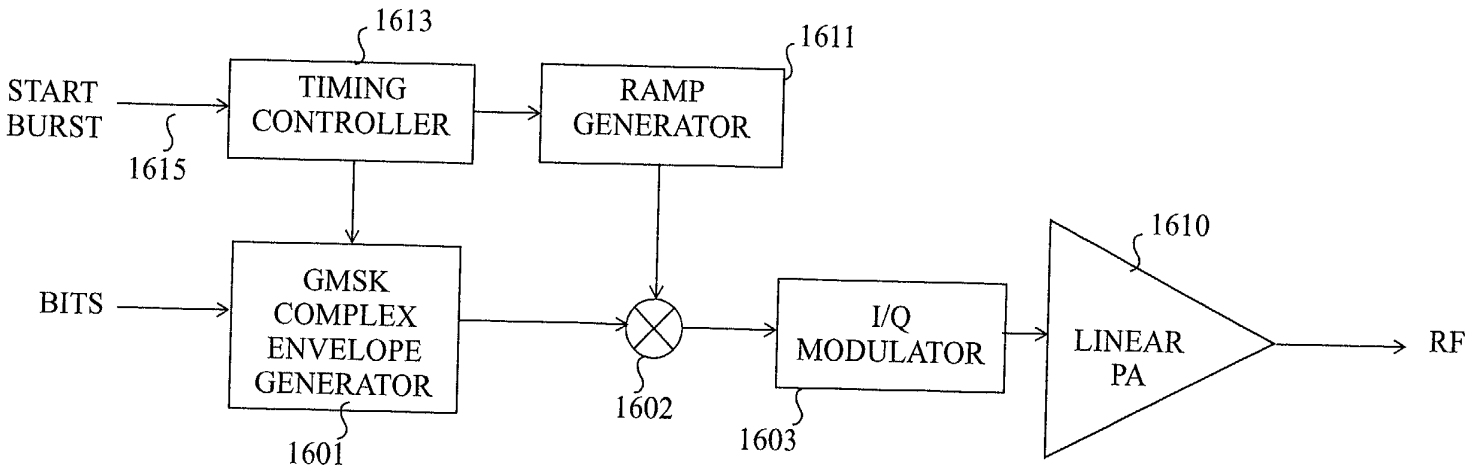


Fig. 16

T0220T "66Tshoot

Fig. 14

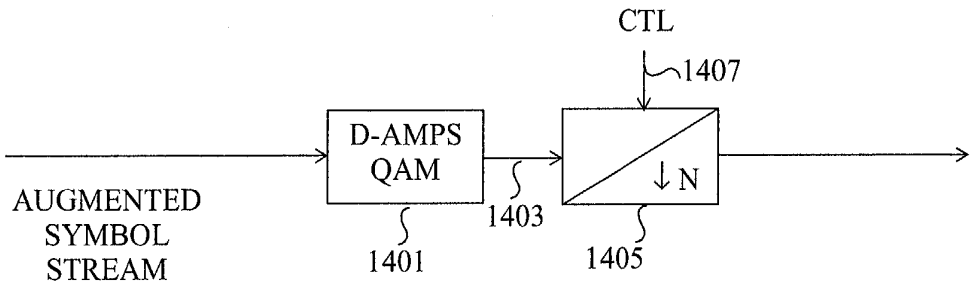
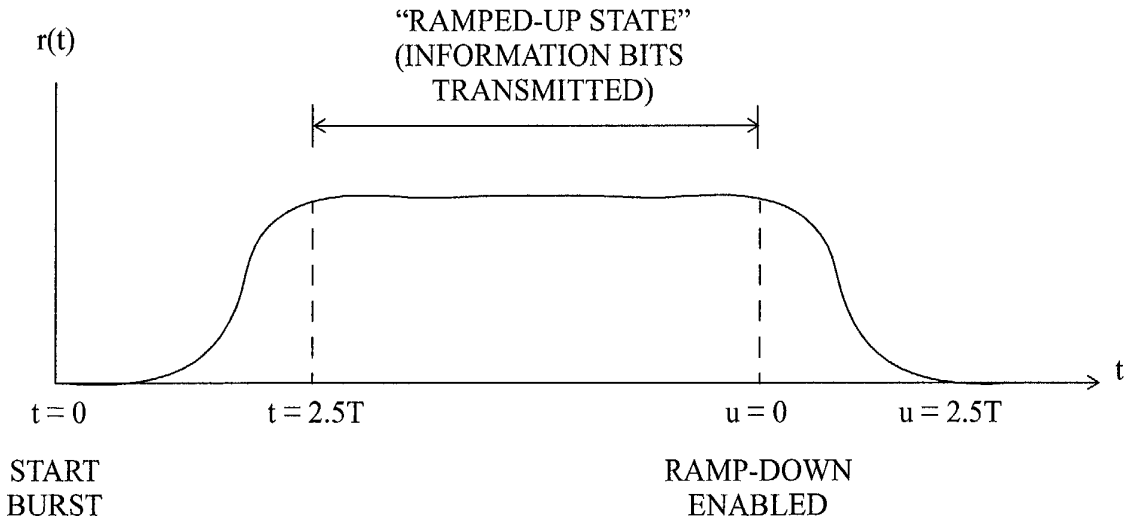


Fig. 17



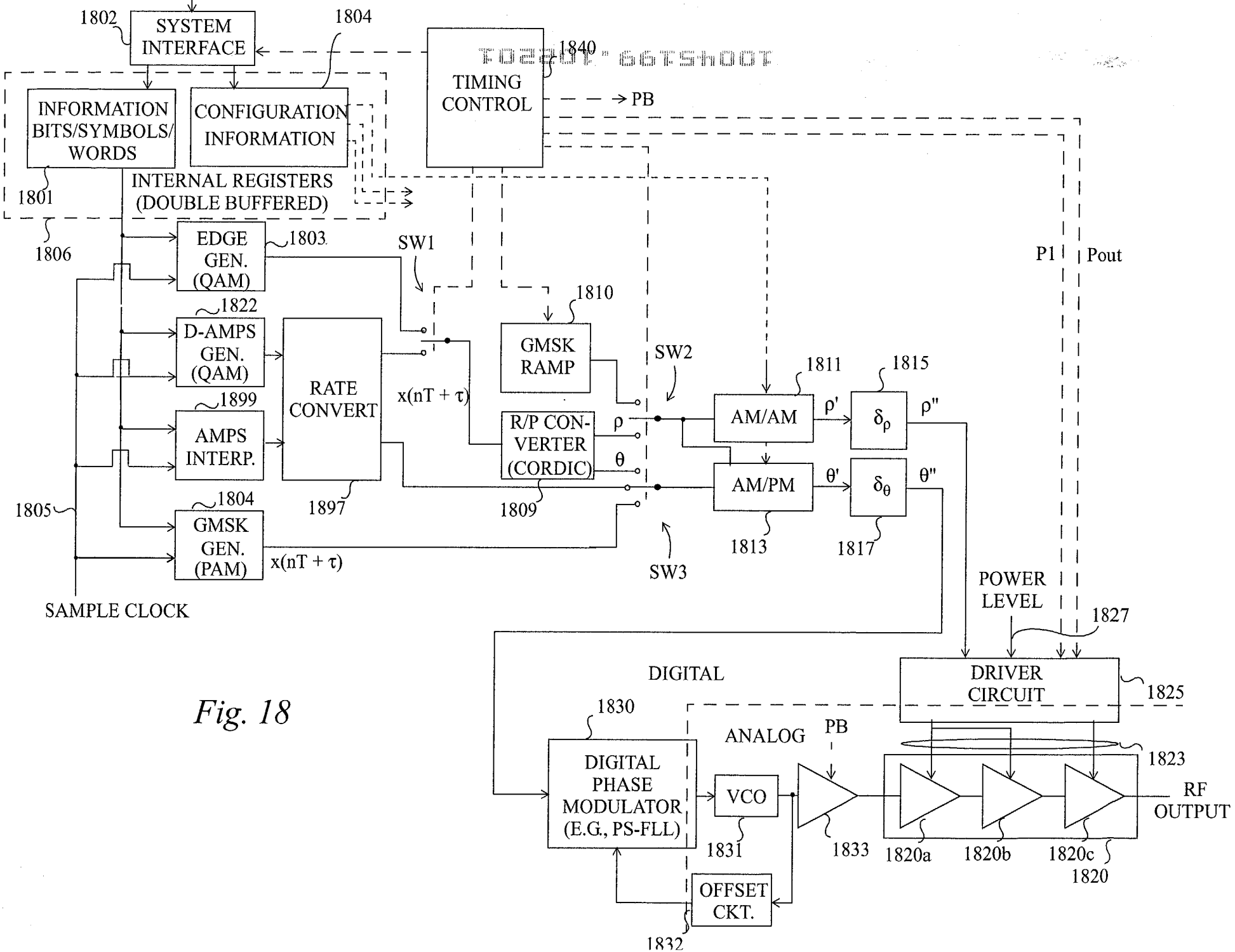

1802
SYSTEM INTERFACE
1804
1840
TIMING CONTROL
PB
INFORMATION BITS/SYMBOLS/ WORDS
CONFIGURATION INFORMATION
1801
INTERNAL REGISTERS (DOUBLE BUFFERED)
1806
EDGE GEN. (QAM)
1803
SW1
P1
Pout
1810
1822
D-AMPS GEN. (QAM)
RATE CONVERT
GMSK RAMP
SW2
1811
1815
1899
AMPS INTERP.
x(nT + τ)
R/P CON-VERTER (CORDIC)
ρ
θ
AM/AM
ρ'
δρ
ρ"
AM/PM
θ'
δθ
θ"
1897
1809
1813
1817
1805
1804
GMSK GEN. (PAM)
x(nT + τ)
SW3
SAMPLE CLOCK
POWER LEVEL
1827
DIGITAL
DRIVER CIRCUIT
1825
1830
ANALOG
PB
DIGITAL PHASE MODULATOR (E.G., PS-FLL)
VCO
1823
RF OUTPUT
1831
1833
1820a
1820b
1820c
1820
OFFSET CKT.
1832

Fig. 18

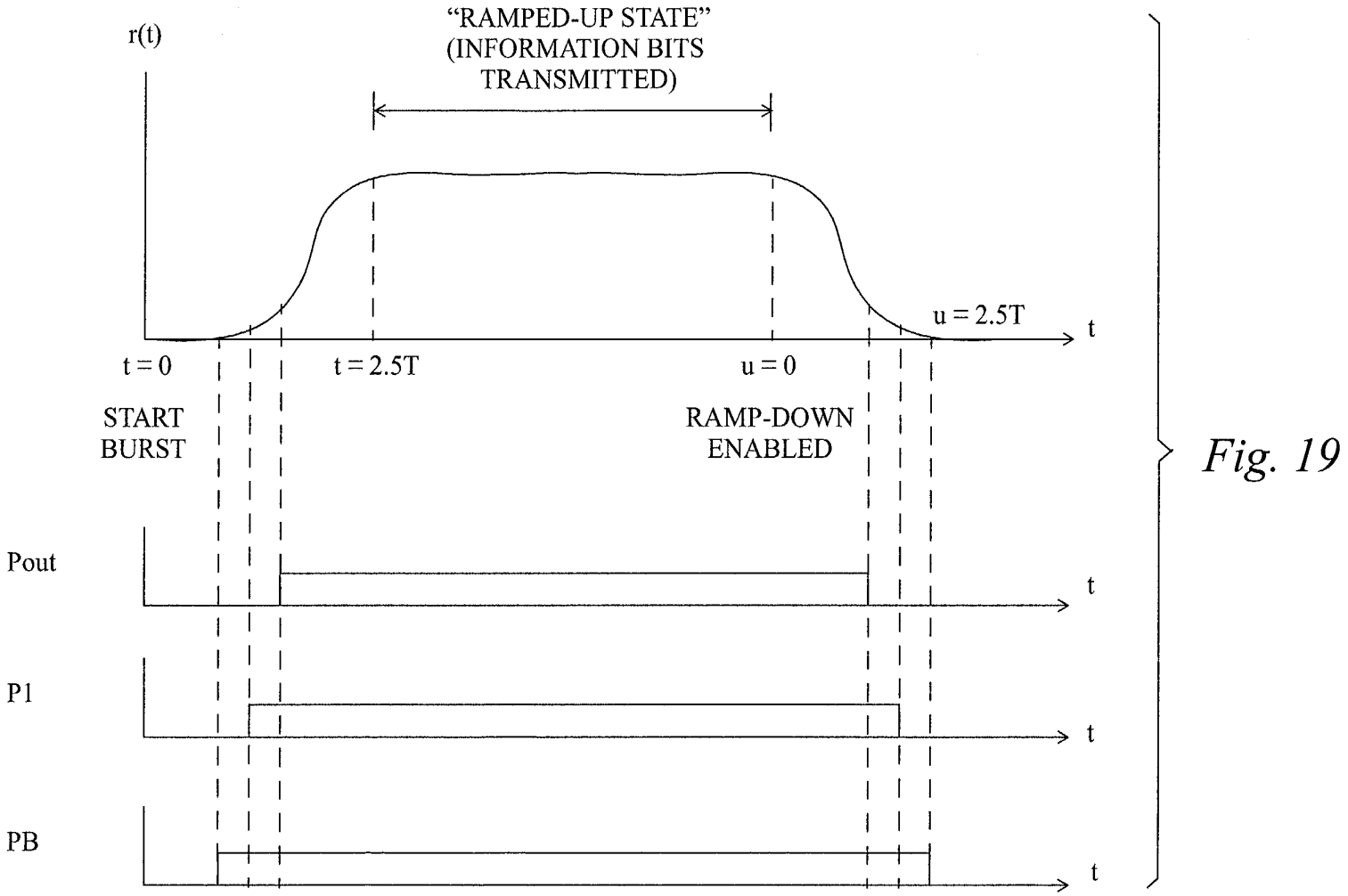

r(t)
"RAMPED-UP STATE"
(INFORMATION BITS
TRANSMITTED)
u = 2.5T
t
t = 0
t = 2.5T
u = 0
START
BURST
RAMP-DOWN
ENABLED
Pout
t
P1
t
PB
t

Fig. 19

T0220T"66T5h00T

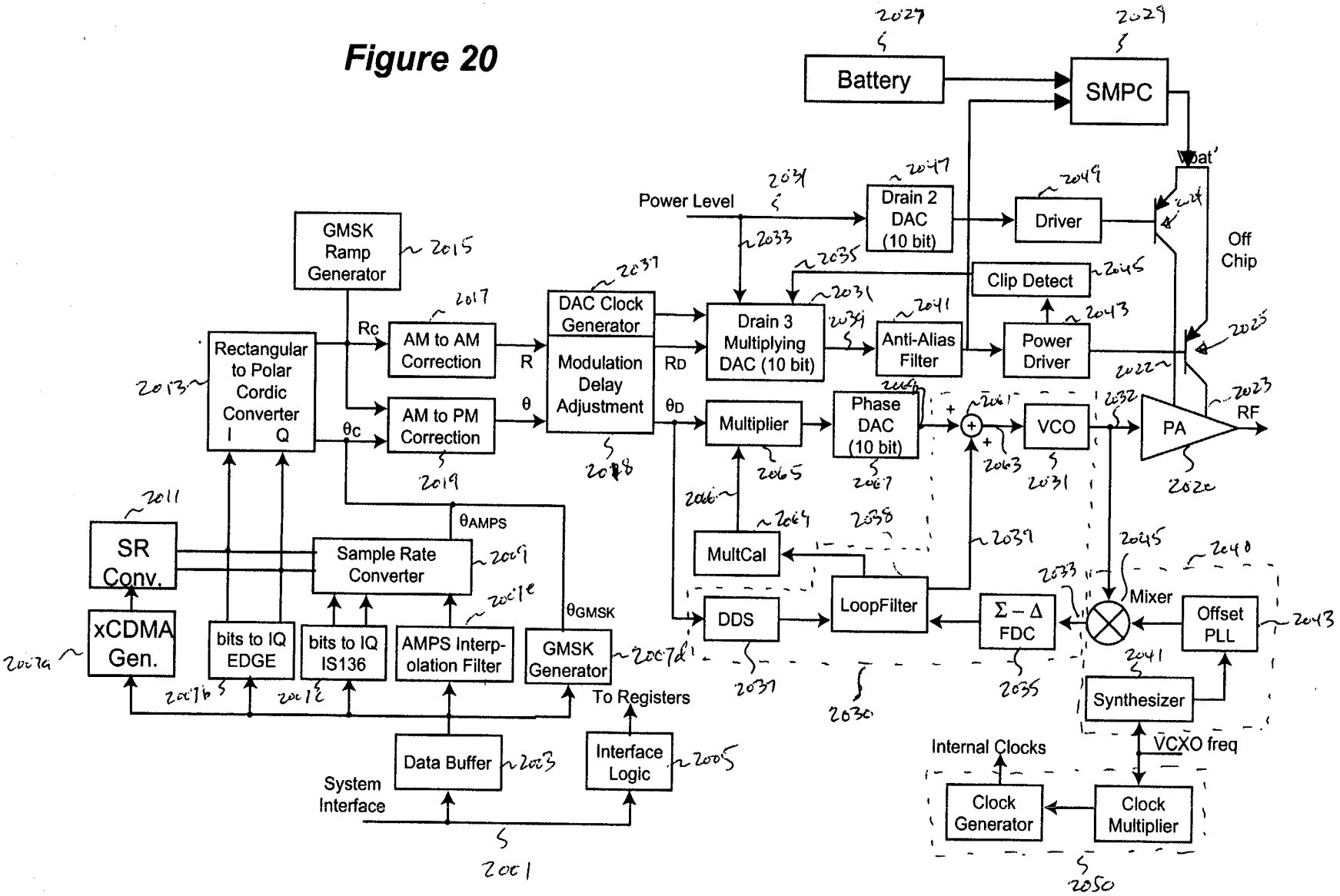



Figure 20